Ordering number : EN*A2279

LC87F2L08A

Advance Information

ON Semiconductor®

http://onsemi.com

CMOS LSI

8-bit Microcontroller

8K-Byte Flash ROM / 256-Byte RAM / 30-pin

Overview

The LC87F2L08A is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrates on a single chip a number of hardware features such as 8K-byte flash ROM (On-board-programmable), 256-byte RAM, an On-chip-debugger, two sophisticated 16-bit timers/counters (may be divided into 8-bit timers), an asynchronous/synchronous SIO interface, a 12/8-bit 9-channel AD converter, four analog comparator, two AMP circuits, an IGBT control circuit(PPG), a watch dog timer, an internal reset a system clock frequency divider, and a 19-source 10-vector interrupt feature.

Features

■ Flash ROM
- 8192 × 8 bits
- Capable of on-board programming with a power voltage range of 4.5 to 5.5V
- Block-erasable in 128 byte units
- Writing in 2-byte units

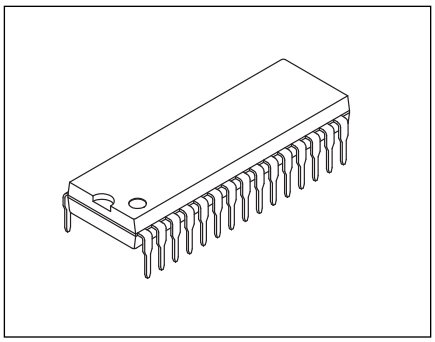
■ ROM
- 256 × 9 bits

■ Package : DIP30SD(400mil), Lead-free type

■ Minimum bus cycle time
- 83.3ns (12MHz)

Note : The bus cycle time here refers to the ROM read speed.

■ Minimum instruction cycle time
- 250ns (12MHz)



DIP30SD(400mil)

* This product is licensed from Silicon Storage Technology, Inc. (USA).

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ORDERING INFORMATION

See detailed ordering and shipping information on page 30 of this data sheet.

■ Ports

- Normal withstand voltage I/O ports
  - Ports I/O direction can be designated in 1 bit units — 9(P14, P15, P20, P21, P30, P70 to P73)
  - Ports I/O direction can be designated in 4 bit units — 8 (P0n)
- Dedicated PPG ports — 7 (PPGO, AMP1I, AMP2O, CMP1IA, CMP1IB, CMP2I, CMP4I)
- Dedicated oscillator ports/input ports — 2 (CF1/XT1, CF2/XT2)
- Reset pin — 1 (RES#)
- Power pins — 3 (VSS1, VSS2, VDD1)

■ Timers

- Timer 0 : 16-bit timer/counter with a capture register.
  - Mode 0 : 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) ×2 channels
  - Mode 1 : 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
  - Mode 2 : 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  - Mode 3 : 16-bit counter (with a 16-bit capture register)
- Timer 1 : 16-bit timer/counter
  - Mode 0 : 8-bit timer with an 8-bit prescaler + 8-bit timer/counter with an 8-bit prescaler
  - Mode 2 : 16-bit timer/counter with an 8-bit prescaler
  - Mode 3 : 16-bit timer with an 8-bit prescaler
- Timer 6 : 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7 : 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
  1) The clock is selectable from the subclock (32.768 kHz crystal oscillation), system clock, and timer 0 prescaler output.
  2) Interrupts are programmable in 5 different time schemes

■ High-speed clock counter

- Can count clocks with a maximum clock rate of 20 MHz (at a main clock of 10 MHz).

■ SIO

- SIO1 : 8-bit asynchronous/synchronous serial interface
  - Mode 0 : Synchronous 8-bit serial I/O (2-wire configuration, 2 to 512 Tcyc transfer clocks)
  - Mode 2 : Bus mode 1 (start bit, 8 data bits, 2 to 512 Tcyc transfer clocks)
  - Mode 3 : Bus mode 2 (start detect, 8 data bits, stop detect)

■ UART

- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2-bit in continuous data transmission)
- Built-in baudrate generator

■ AD converter : 12 bits/8 bits × 9 channels

- 12/8 bits AD converter resolution selectable

■ Remote control receiver circuit (sharing pins with P73, INT3, and T0IN)

- Noise rejection function (noise filter time constant selectable from 1Tcyc/32Tcyc/128Tcyc)

■ Clock output function

- Can generate clock outputs with a frequency of $\frac{1}{1}$, $\frac{1}{2}$, $\frac{1}{4}$, $\frac{1}{8}$, $\frac{1}{16}$, $\frac{1}{32}$, $\frac{1}{64}$ of the source clock selected as the system clock.
- Can generate the source clock for the subclock.

■ Analog comparator × 4 channels

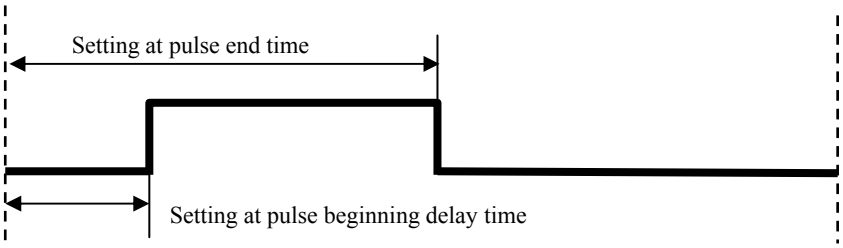
- CMP1 : Both input terminals of "+" and "-".
  Output: For timing generation of PPG output and capture timer input(INT2).
- CMP2 : Input terminal of "+", "-" input is 2/3VDD of internal Vref.
  Interrupt flag set of output (INT0).
- CMP 3: "+" input is output of AMP1. "-" input is 2/3VDD of internal Vref.
  PPG output control of CMP3 output (OFF only at a present cycle) and interrupt flag set (INT1).
- CMP4 : Input terminal of "+", "-" input is 2/3VDD of internal Vref.
  PPG output control of CMP4 output (compulsion OFF) and interrupt flag set(CMP4).

■ AMP circuit × 2 channels

- AMP1 : The magnification is set by the user option (×6/×8/×10).
  Input terminal (AMP1I)
  Output is CMP3 input and AMP2 input.
- AMP2 : The magnification is set by the register (×1/×2/×4).
  Input is AMP1 output.
  Output rerminal (AMP2O)

■ Pulse output control circuit (PPG output) × 1 channels

- Output synchronous signal switch : Set by the register (1 pulse output) / Continuous pulse output of synchronizationto CMP1 output .
- Duty control : The pulse beginning delay time and the pulse end time form synchronous idle are set according to the register.
- PPG output is compulsion OFF by the CMP3/CMP4 output.
- CMP1 output : Timing detection of pulse signal.
- The output polarity can be switched : User option setting.



■ Watchdog timer

- Can generate the internal reset signal on a timer overflow monitored by the WDT-dedicated low-speed RC oscillation clock (30kHz).
- Allows selection of continue, stop, or hold mode operation of the counter on entry into the HALT/ HOLD mode.

■ Interrupts

- 19 sources, 10 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	UART1 receive
8	0003BH	H or L	SIO1/UART1 transmit
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/CMP4

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■ Subroutine stack levels: 128levels (the stack is allocated in RAM.)

■ High-speed multiplication/division instructions

- 16 bits × 8 bits (5 Tcyc execution time)
- 24 bits × 16 bits (12 Tcyc execution time)
- 16 bits ÷ 8 bits (8 Tcyc execution time)
- 24 bits ÷ 16 bits (12 Tcyc execution time)

■ Oscillation circuits

- Internal oscillation circuits
  Low-speed RC oscillation circuit 1 : For system clock(100kHz)
  Medium-speed RC oscillation circuit : For system clock(1MHz)
  Multifrequency RC oscillation circuit : For system clock(8MHz)
  Low-speed RC oscillation circuit 2 : For watch dog timer(30kHz)
- External oscillation circuits
  Hi-speed CF oscillation circuit : For system clock, with internal Rf
  Low speed crystal oscillation circuit : For low-speed system clock, with internal Rf
  1) The CF and crystal oscillation circuits share the same pins. The active circuit is selected under program control.
  2) Both the CF and crystal oscillator circuits stop operation on a system reset. When the reset is released, only the CF oscillation circuit resumes operation.

■ System clock divider function

- Can run on low current.
- The minimum instruction cycle selectable from 300 ns, 600 ns, 1.2 μs, 2.4 μs, 4.8 μs, 9.6 μs, 19.2 μs, 38.4 μs, and 76.8 μs (at a main clock rate of 10 MHz).

■ Internal reset function

- Power-on reset (POR) function
  1) POR reset is generated only at power-on time.
  2) The POR release level can be selected from 8 levels (1.67V, 1.97V, 2.07V, 2.37V, 2.57V, 2.87V, 3.86V, and 4.35V) through option configuration.
- Low-voltage detection reset (LVD) function
  1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  2) The use/disuse of the LVD function and the low voltage threshold level (7 levels: 1.91V, 2.01V, 2.31V, 2.51V, 2.81V, 3.79V, 4.28V).

■ Standby function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) There are three ways of resetting the HALT mode.
     (1) Setting the reset pin to the low level
     (2) System resetting by watchdog timer or low-voltage detection
     (3) Occurrence of an interrupt

- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The CF, RC, and crystal oscillators automatically stop operation.
  2) There are four ways of resetting the HOLD mode.
     (1) Setting the reset pin to the lower level.
     (2) System resetting by watchdog timer or low-voltage detection
     (3) Having an interrupt source established at either INT0, INT1, INT2, INT4 or INT5
         * INT0 and INT1 HOLD mode reset is available only when level detection is set.
     (4) Having an interrupt source established at port 0.

- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  1) The CF and RC oscillators automatically stop operation.
  2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are five ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level.
     (2) System resetting by watchdog timer or low-voltage detection.
     (3) Having an interrupt source established at either INT0, INT1, INT2, INT4 or INT5
         * INT0 and INT1 HOLD mode reset is available only when level detection is set.
     (4) Having an interrupt source established at port 0.
     (5) Having an interrupt source established in the base timer circuit.

  Note: Available only when X’tal oscillation is selected.

■ On-chip debugger

- Supports software debugging with the IC mounted on the target board.

■ Data security function (flash versions only)

- Protects the program data stored in flash memory from unauthorized read or copy.
  Note : This data security function does not necessarily provide absolute data security.

■ Development tools

- On-chip-debugger : TCB87 TypeB + LC87F2L08A

■ Programming board

Package	Programming board
DIP30SD	W87F2LD

■ Flash ROM programmer

Maker		Model	Supported version	Device
Flash Support Group, Inc. (FSG)	Single Programmer	AF9708 AF9709/AF9709B/AF9709C (Including Ando Electric Co., Ltd. models)	Rev03.12	LC87F2L08A
	Gang Programmer	AF9723/AF9723B(Main body) (Including Ando Electric Co., Ltd. models)	*1	LC87F2L08A
		AF9833(Unit) (Including Ando Electric Co., Ltd. models)	*1	
ON Semiconductor	Single/Gang Programmer	SKK/SKK Type B (SanyoFWS)	Application Version 1.04 or later Chip Data Version 2.18 or later	LC87F2L08
	Gang Programmer	SKK-4G (SanyoFWS)		
	In-circuit/Gang Programmer	SKK-DBG Type B (SanyoFWS)		

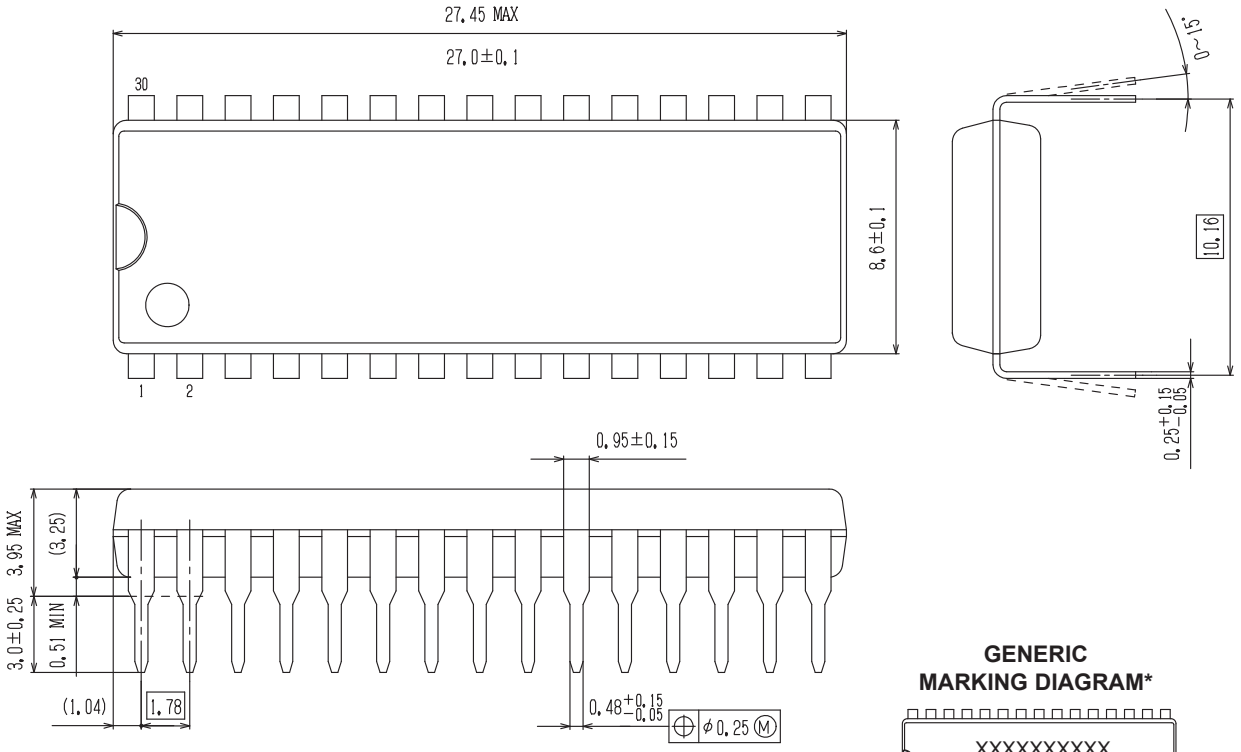
Note : Check for the latest version.
*1 : We have a schedule to request the registration.

For information about AF-Series:
Flash Support Group, Inc.
TEL: +81-53-459-1050
E-mail: sales@j-fsg.co.jp

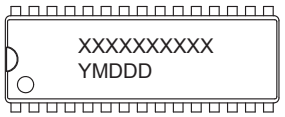
Package Dimensions

unit : mm

PDIP30 / DIP30SD (400 mil)
CASE 646AZ
ISSUE A



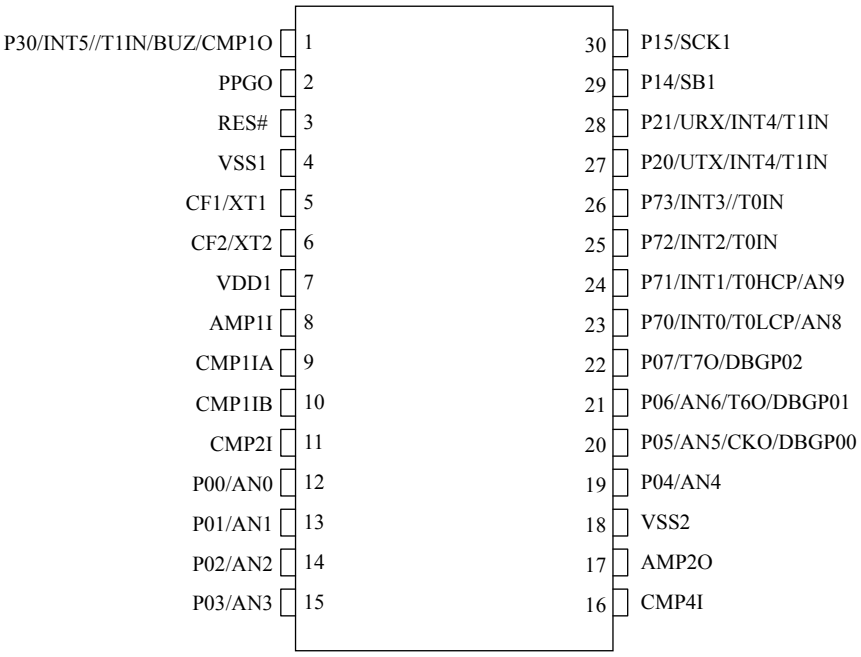
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

Pin Assignment

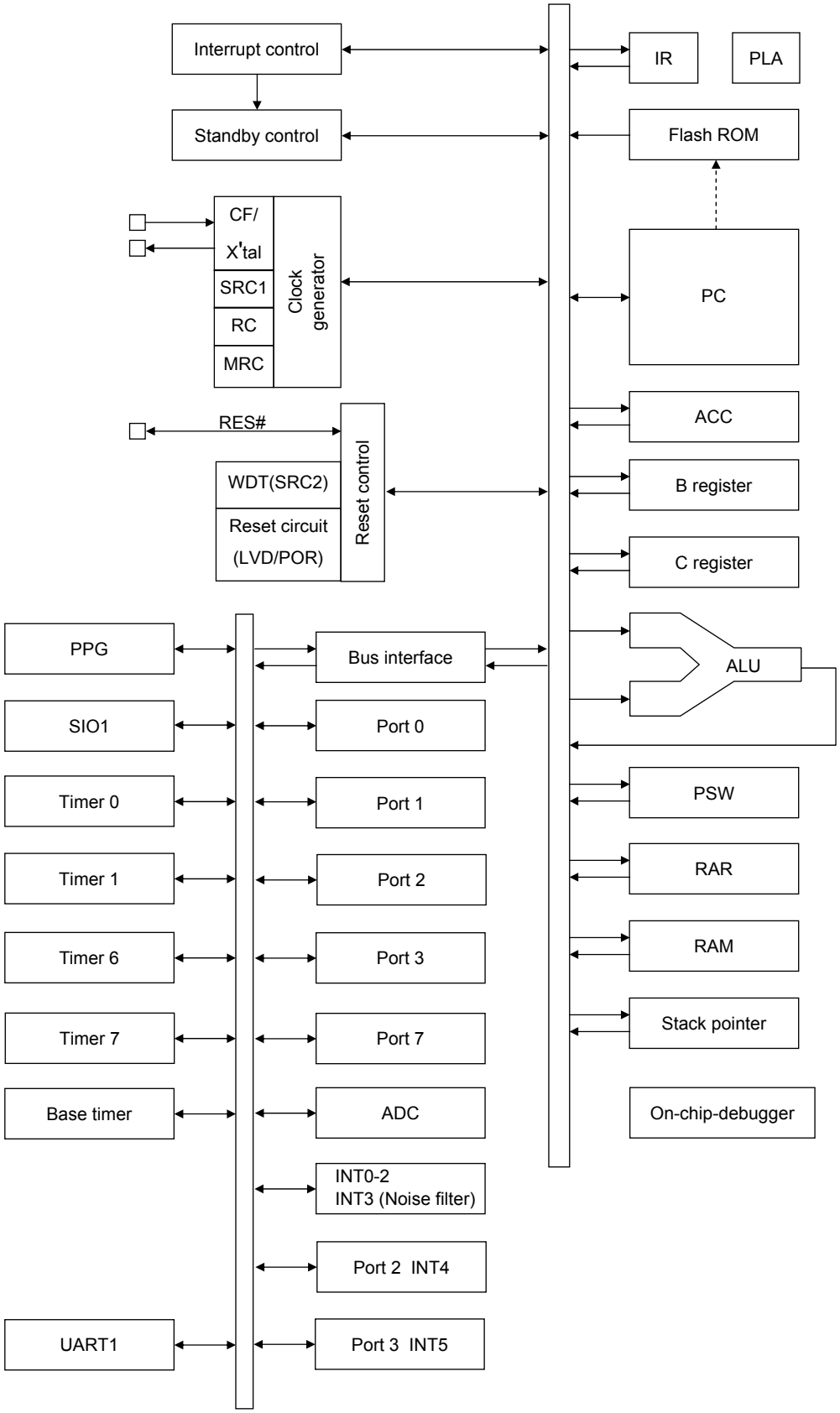


DIP30SD “Lead-free Type”

DIP30SD	NAME
1	P30/INT5//T1IN/BUZ/CMP1O
2	PPGO
3	RES#
4	VSS1
5	CF1/XT1
6	CF2/XT2
7	VDD1
8	AMP1I
9	CMP1IA
10	CMP1IB
11	CMP2I
12	P00/AN0
13	P01/AN1
14	P02/AN2
15	P03/AN3

DIP30SD	NAME
16	CMP4I
17	AMP2O
18	VSS2
19	P04/AN4
20	P05/AN5/CKO/DBGP00
21	P06/AN6/T6O/DBGP01
22	P07/T7O/DBGP02
23	P70/INT0/T0LCP/AN8
24	P71/INT1/T0HCP/AN9
25	P72/INT2/T0IN
26	P73/INT3//T0IN
27	P20/UTX/INT4/T1IN
28	P21/URX/INT4/T1IN
29	P14/SB1
30	P15/SCK1

System Block Diagram



Pin Function Chart

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>VSS1
VSS2</td><td>–</td><td>– power supply pins</td><td>No</td></tr>
<tr><td>VDD1</td><td>–</td><td>+ power supply pin</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 4 bit units
• Pull-up resistors can be turned on and off in 4 bit units.
• HOLD reset input
• Port 0 interrupt input
• Pin functions
P05: System clock output
P06: Timer 6 toggle output
P07: Timer 7 toggle output
P00(AN0) to P06(AN6):AD converter input
P05(DBGP00) to P07(DBGP02):On-chip debugger port</td><td>Yes</td></tr>
<tr><td>Port 1
P14 to P15</td><td>I/O</td><td>• 2-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
• Pin functions
P14: SIO1 data I/O
P15: SIO1 clock I/O</td><td>Yes</td></tr>
<tr><td>Port 2
P20 to P21</td><td>I/O</td><td>• 2-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
• Pin functions
P20 : UART transmit
P21 : UART receive
P20 to P21 : INT4 input / HOLD reset input / timer 1 event input / timer 0L capture input / timer 0H capture input
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 3
P30</td><td>I/O</td><td>• 1-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
• Pin functions
P30: BUZ output/CMP1O output/ INT5 input/HOLD reset input / timer 1 event input / timer 0L capture input/timer 0H capture input
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT5</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr>
</table></td><td>Yes</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7
P70 to P73</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
• Pin functions
P70 : INT0 input / HOLD reset input / timer 0L capture input
P71 : INT1 input / HOLD reset input / timer 0H capture input
P72 : INT2 input / HOLD reset input / timer 0 event input / timer 0L capture input
P73 : INT3 input (with noise filter) / timer 0 event input / timer 0H capture input
P70(AN8),P71(AN9) : AD converter input
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>○</td><td>○</td><td>×</td><td>○</td><td>○</td></tr>
<tr><td>INT1</td><td>○</td><td>○</td><td>×</td><td>○</td><td>○</td></tr>
<tr><td>INT2</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr>
<tr><td>INT3</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr>
</table></td><td>No</td></tr>
<tr><td>AMP1I</td><td>I</td><td>AMP1 input</td><td>No</td></tr>
<tr><td>AMP2O</td><td>O</td><td>AMP2 output</td><td>No</td></tr>
<tr><td>CMP1IA</td><td>I</td><td>CMP1 input(-)</td><td>No</td></tr>
<tr><td>CMP1IB</td><td>I</td><td>CMP1 input(+)</td><td>No</td></tr>
<tr><td>CMP2I</td><td>I</td><td>CMP2 input(+)</td><td>No</td></tr>
<tr><td>CMP4I</td><td>I</td><td>CMP4 input(+)</td><td>No</td></tr>
<tr><td>PPGO</td><td>O</td><td>PPG output</td><td>Yes</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I/O</td><td>External reset Input / internal reset output</td><td>No</td></tr>
<tr><td>CF1/XT1</td><td>I</td><td>• Ceramic resonator or 32.768kHz crystal oscillator input pin
• Pin function
General-purpose input port</td><td>No</td></tr>
<tr><td>CF2/XT2</td><td>I/O</td><td>• Ceramic resonator or 32.768kHz crystal oscillator output pin
• Pin function
General-purpose input port</td><td>No</td></tr>
</table>

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port Name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P14 to P15 P20 to P21 P30	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P31	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	–	No	Nch-open drain	Programmable
P71 to P73	–	No	CMOS	Programmable
PPGO	–	1	CMOS	No
		2	Nch-open drain	No

Note 1 : The control of the presence or absence of the programmable pull-up resistors for port 0 and the switching between low- and high-impedance pull-up connection is exercised in nibble (4-bit) units (P00 to 03 or P04 to 07).

User Option Table

Option name	Option to be applied on	Flash-ROM version	Option selected in units of	Option selection
Port output type	P00 to P07	○	1 bit	CMOS
				Nch-open drain
	P14 to P15	○	1 bit	CMOS
				Nch-open drain
	P20 to P21	○	1 bit	CMOS
				Nch-open drain
	P30	○	1 bit	CMOS
				Nch-open drain
	PPGO	○	-	CMOS
				Nch-open drain
PPGO output polarity	PPGO	○	-	Not inverted
				Inverted
Magnification of AMP1	-	○	-	x6
				x8
				x10
Program start address	-	○	-	00000h
				01E00h
Low-voltage detection reset function	Detect function	○	-	Enable : Use
				Disable : Not Used
	Detect level	○	-	7-level
Power-on reset function	Power-On reset level	○	-	8-level

Recommended Unused Pin Connections

Pin Name	Recommended Unused Pin Connections	
	Board	Software
P00 to P07	Open	Output low
P14 to P15	Open	Output low
P20 to P21	Open	Output low
P30	Open	Output low
P70 to P73	Open	Output low
CF1/XT1	Pulled low with a 100kΩ resistor or less	General-purpose input port
CF2/XT2	Pulled low with a 100kΩ resistor or less	General-purpose input port

On-chip Debugger pin connection requirements

For the treatment of the on-chip debugger pins, refer to the separately available documents entitled "RD87 Onchip Debugger Installation Manual" and "LC872000 Series Onchip debugger pin connection requirements"

Note : Be sure to electrically short-circuit between the VSS1 and VSS2 pins.

1. Absolute Maximum Ratings at Ta=25°C, $V_{SS}1$= $V_{SS}2$= 0V

Parameter		Symbol	Pin/Remarks	Conditions	VDD[V]	Specification min.	typ.	max.	unit
Maximum supply voltage		VDDMAX	VDD1			−0.3	–	+6.5	V
Input voltage		VI	CF1, RES#, AMP1I, CMP1IA,CMP1IB, CMP2I, CMP4I			−0.3	–	VDD+0.3	
output voltage		VO	AMP2O, PPGO			−0.3	–	VDD+0.3	
Input/output voltage		VIO	CF2, Ports 0, 1, 2, 3, Port 7			−0.3	–	VDD+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2, 3, PPGO	CMOS output select Per 1 applicable pin		−10			mA
		IOPH(2)	P71 to P73	Per 1 applicable pin		−5			
	Mean output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2, 3, PPGO	CMOS output select Per 1 applicable pin		−7.5			
		IOMH(2)	P71 to P73	Per 1 applicable pin		−3			
	Total output current	ΣIOAH(1)	P71 to P73	Total of all applicable pins		−10			
		ΣIOAH(2)	Ports 0, 1, 2, 3, PPGO	Total of all applicable pins		−25			
Low level output current	Peak output current	IOPL(1)	P02 to P07, Ports 1, 2, 3, PPGO	Per 1 applicable pin				20	
		IOPL(2)	P00, P01	Per 1 applicable pin				30	
		IOPL(3)	Port 7	Per 1 applicable pin				10	
	Mean output current (Note 1-1)	IOML(1)	P02 to P07, Ports 1, 2, 3, PPGO	Per 1 applicable pin				15	
		IOML(2)	P00, P01	Per 1 applicable pin				20	
		IOML(3)	Port 7	Per 1 applicable pin				7.5	
	Total output current	ΣIOAL(1)	P00 to P03	Total of all applicable pins				40	
		ΣIOAL(2)	P04 to P07, Ports 1, 2, 3, 7, PPGO	Total of all applicable pins				40	
		ΣIOAL(3)	Ports 0, 1, 2, 3, 7, PPGO	Total of all applicable pins				70	
Power dissipation		Pdmax(1)	DIP30SD	Ta=−40 to +85°C Package only				350	mW
		Pdmax(2)		Ta=−40 to +85°C Package with thermal resistance board (Note 1-2)				540	
Operating ambient temperature		Topr				−40	–	+85	°C
Storage ambient temperature		Tstg				−55	–	+125	

Note 1-1 : The mean output current is a mean value measured over 100ms.
Note 1-2 : SEMI standards thermal resistance board (size : 76.1×114.3×1.6tmm, glass epoxy) is used.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Allowable Operating Conditions at Ta=–40 to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	VDD[V]	Specification min.	typ.	max.	unit
Operating supply voltage (Note 2-1)	VDD	VDD1	0.245µs ≤ tCYC ≤ 200µs		4.5		5.5	V
Memory sustaining supply voltage	VHD	VDD1	RAM and register contents sustained in HOLD mode.		2.0			
High level input voltage	VIH(1)	Ports 1, 2, 3, 7		4.5 to 5.5	0.3VDD +0.7		VDD	
	VIH(2)	Ports 0		4.5 to 5.5	0.3VDD +0.7		VDD	
	VIH(3)	CF1, RES#		4.5 to 5.5	0.75VDD		VDD	
Low level input voltage	VIL(1)	Ports 1, 2, 3, 7		4.5 to 5.5	VSS		0.1VDD +0.4	
	VIL(2)	Ports 0		4.5 to 5.5	VSS		0.15VDD +0.4	
	VIL(3)	CF1, RES#		1.8 to 5.5	VSS		0.25VDD	
Instruction cycle time (Note 2-1)	tCYC (Note 2-2)			4.5 to 5.5	0.245		200	µs
External system clock frequency	FEXCF	CF1	• CF2 pin open • System clock frequency division ratio = 1/1 • External system clock duty = 50±5%	4.5 to 5.5	0.1		12	MHz
			• CF2 pin open • System clock frequency division ratio = 1/2 • External system clock duty = 50±5%	4.5 to 5.5	0.2		24.4	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	12 MHz ceramic oscillation See Fig. 1.	4.5 to 5.5		12		MHz
	FmCF(2)	CF1, CF2	10 MHz ceramic oscillation See Fig. 1.	4.5 to 5.5		10		
	FmCF(3)	CF1, CF2	4 MHz ceramic oscillation. CF oscillation normal amplifier size selected. See Fig. 1. (CFLAMP=0)	4.5 to 5.5		4		
			4 MHz ceramic oscillation. CF oscillation low amplifier size selected. (CFLAMP=1) See Fig. 1.	4.5 to 5.5		4		
	FmMRC		Frequency variable RC oscillation. 1/2 frequency division ratio. (RCCTD=0) (Note 2-4)	4.5 to 5.5	7.44	8.0	8.56	
	FmRC		Internal Medium-speed RC oscillation	4.5 to 5.5	0.5	1.0	2.0	
	FmSRC1		Internal Low-speed RC oscillation 1	4.5 to 5.5	50	100	200	kHz
	FmSRC2		Internal Low-speed RC oscillation 2	4.5 to 5.5	15	30	60	
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 2.	4.5 to 5.5		32.768		

Note 2-1 : V_{DD} must be held greater than or equal to 2.2 V in the flash ROM onboard programming mode.

Note 2-2 : Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3 : See Tables 1 and 2 for the oscillation constants.

Note 2-4 : When switching the system clock, allow an oscillation stabilization time of 100 µs or longer after the multifrequency RC oscillator circuit transmits from the "oscillation stopped" to "oscillation enabled" state.

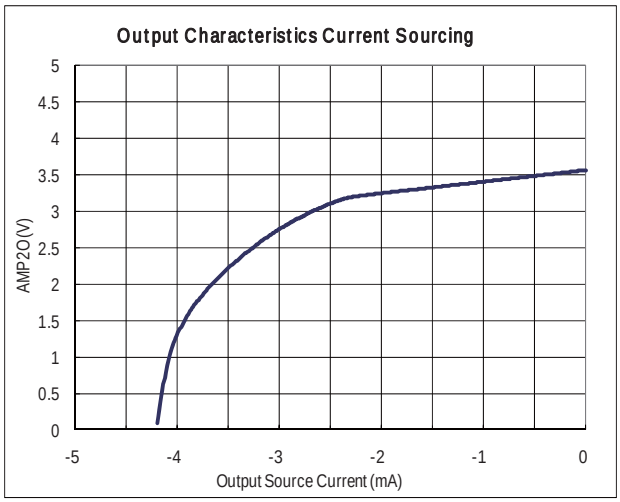
Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

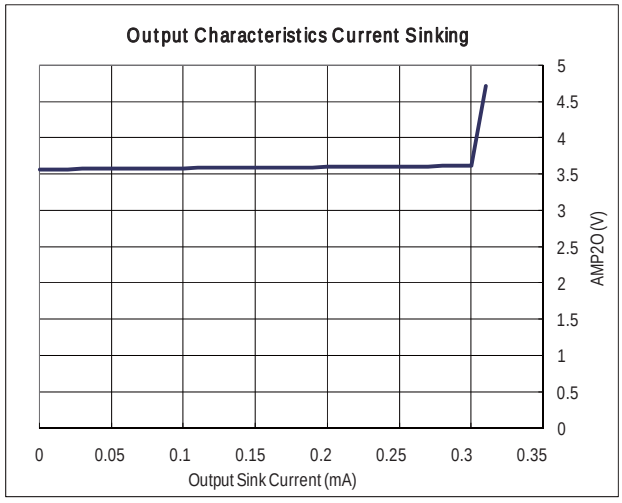
3. Electrical Characteristics at Ta=–40 to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	VDD[V]	Specification min.	typ.	max.	unit
High level input current	IIH(1)	Ports 0, 1, 2, 3 Ports 7, CMP1IA, CMP1IB, CMP2I, CMP4I, AMP1I, RES#	Output disabled Pull-up resistor off VIN=VDD (Including output Tr's off leakage current)	4.5 to 5.5			1	µA
	IIH(2)	CF1	VIN=VDD	4.5 to 5.5			15	
Low level input current	IIL(1)	Ports 0, 1, 2, 3 Ports 7, CMP1IA, CMP1IB, CMP2I, CMP4I, AMP1I, RES#	Output disabled Pull-up resistor off VIN=VSS (Including output Tr's off leakage current)	4.5 to 5.5	–1			
	IIL(2)	CF1	VIN=VSS	4.5 to 5.5	–15			
AMP output current (Note 3-1)	IAMPO	AMP2O	Magnification of AMP1 is selected x8 by user option Magnification of AMP2 is selected x1 by resister AMP1I=0.445V	5.0	–2.3		0.30	mA
High level output voltage	VOH(1)	Ports 0, 1, 2 P71 to P73	IOH=–1mA	4.5 to 5.5	VDD–1			V
	VOH(4)	Port 3,PPGO	IOH=–6mA	4.5 to 5.5	VDD–1			
Low level output voltage	VOL(1)	Ports 0, 1, 2, 3, PPGO	IOL=10mA	4.5 to 5.5			1.5	
	VOL(2)		IOL=1.4mA	4.5 to 5.5			0.4	
	VOL(4)	Port 7	IOL=1.4mA	4.5 to 5.5			0.4	
	VOL(6)	P00, P01	IOL=25mA	4.5 to 5.5			1.5	
	VOL(7)		IOL=4mA	4.5 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Ports 0, 1, 2, 3 Port 7	VOH=0.9VDD When Port 0 selected low-impedance pull-up.	4.5 to 5.5	18	50	230	kΩ
	Rpu(3)	Port 0	VOH=0.9VDD When Port 0 selected High-impedance pull-up.	4.5 to 5.5	100	210	400	
Hysteresis voltage	VHYS(1)	Ports 1, 2, 3, 7, RES#		4.5 to 5.5		0.1 VDD		V
Pin capacitance	CP	All pins	For pins other than that under test: VIN=VSS f=1MHz Ta=25°C	4.5 to 5.5		10		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Note 3-1 :





4. Serial I/O Characteristics at Ta=–40 to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

4-1. SIO1 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/Remarks	Conditions	VDD[V]	Specification min.	typ.	max.	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	• See Fig. 5.	4.5 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 5.	4.5 to 5.5	2			
		Low level pulse width	tSCKL(4)				1/2			tSCK
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 5.	4.5 to 5.5	0.05			µs
	Data hold time		thDI(2)				0.05			
Serial output	Output delay time		tdD0(4)	SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 5.	4.5 to 5.5			(1/3)tCYC +0.08	

Note 4-1-1 : These specifications are theoretical values. Add margin depending on its use.

5. Pulse Input Conditions at Ta=–40 to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	VDD[V]	Specification min.	typ.	max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P21), INT5(P30 to P31)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	4.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	4.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	4.5 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	4.5 to 5.5	256			
	tPIL(5)	RES#	• Resetting is enabled.	4.5 to 5.5	200			µs

6. AD Converter Characteristics at $V_{SS}1= V_{SS}2=0V$

<12bits AD Converter Mode / Ta=–40 to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions	VDD[V]	Specification min.	typ.	max.	unit
Resolution	N	AN0(P00) to AN6(P06) AN8(P70) AN9(P71)		4.5 to 5.5		12		bit
Absolute accuracy	ET		(Note 6-1)	4.5 to 5.5			±16	LSB
Conversion time	TCAD		• See Conversion time calculation formulas. (Note 6-2)	4.5 to 5.5	32		115	μs
Analog input voltage range	VAIN			4.5 to 5.5	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 to 5.5			1	μA
	IAINL		VAIN=VSS	4.5 to 5.5	–1			

<8bits AD Converter Mode / Ta=–40 to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions	VDD[V]	Specification min.	typ.	max.	unit
Resolution	N	AN0(P00) to AN6(P06) AN8(P70) AN9(P71)		4.5 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	4.5 to 5.5			±1.5	LSB
Conversion time	TCAD		• See Conversion time calculation formulas. (Note 6-2)	4.5 to 5.5	20		90	μs
Analog input voltage range	VAIN			4.5 to 5.5	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 to 5.5			1	μA
	IAINL		VAIN=VSS	4.5 to 5.5	–1			

Conversion time calculation formulas :

12bits AD Converter Mode : TCAD(Conversion time)=((52/(AD division ratio))+2)×(1/3)×tCYC

8bits AD Converter Mode : TCAD(Conversion time)=((32/(AD division ratio))+2)×(1/3)×tCYC

External oscillation (FmCF)	Operating supply voltage range (VDD)	System division ratio (SYSDIV)	Cycle time (tCYC)	AD division ratio (ADDIV)	AD conversion time (TCAD) 12bit AD	8bit AD
CF-12MHz	4.5V to 5.5V	1/1	250ns	1/8	34.8μs	21.5μs
CF-10MHz	4.5V to 5.5V	1/1	300ns	1/8	41.8μs	25.8μs
CF-4MHz	4.5V to 5.5V	1/1	750ns	1/8	104.5μs	64.5μs

Note 6-1 : The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2 : The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

7. Power-on Reset (POR) Characteristics at Ta=–40 to +85°C, $V_{SS}1= V_{SS}2=0V$

Parameter	Symbol	Pin/Remarks	Conditions	Option selected voltage	Specification min.	typ.	max.	unit
POR release voltage	PORRL		• Select from option. (Note 7-1)	1.67V	1.55	1.67	1.79	V
				1.97V	1.85	1.97	2.09	
				2.07V	1.95	2.07	2.19	
				2.37V	2.25	2.37	2.49	
				2.57V	2.45	2.57	2.69	
				2.87V	2.75	2.87	2.99	
				3.86V	3.73	3.86	3.99	
				4.35V	4.21	4.35	4.49	
Detection voltage unknown state	POUKS		• See Fig. 7. (Note 7-2)			0.7	0.95	
Power supply rise time	PORIS		• Power supply rise time from 0V to 1.6V.				100	ms

Note7-1 : The POR release level can be selected out of 8 levels only when the LVD reset function is disabled.
Note7-2 : POR is in an unknown state before transistors start operation.

8. Low Voltage Detection Reset (LVD) Characteristics at Ta=–40 to +85°C, $V_{SS}1= V_{SS}2=0V$

Parameter	Symbol	Pin/Remarks	Conditions	Option selected voltage	Specification min.	typ.	max.	unit
LVD reset Voltage (Note 8-2)	LVDET		• Select from option. (Note 8-1) (Note 8-3) • See Fig. 8.	1.91V	1.81	1.91	2.01	V
				2.01V	1.91	2.01	2.11	
				2.31V	2.21	2.31	2.41	
				2.51V	2.41	2.51	2.61	
				2.81V	2.71	2.81	2.91	
				3.79V	3.69	3.79	3.89	
				4.28V	4.18	4.28	4.38	
LVD hysteresis width	LVHYS			1.91V		55		mV
				2.01V		55		
				2.31V		55		
				2.51V		55		
				2.81V		60		
				3.79V		65		
				4.28V		65		
Detection voltage unknown state	LVUKS		• See Fig. 8. (Note 8-4)			0.7	0.95	V
Low voltage detection minimum width (Reply sensitivity)	TLVDW		• LVDET-0.5V • See Fig. 9.		0.2			ms

Note8-1 : The LVD reset level can be selected out of 7 levels only when the LVD reset function is enabled.
Note8-2 : LVD reset voltage specification values do not include hysteresis voltage.
Note8-3 : LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.
Note8-4 : LVD is in an unknown state before transistors start operation.

9. Amplifier and Comparator Characteristics at Ta=–40 to +85°C, $V_{SS}1= V_{SS}2=0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				VDD[V]	min.	typ.	max.	unit
Input common-mode voltage (Note9-1)	VCMIN	CMP1IA, CMP1IB, CMP2I,CMP4I		4.5 to 5.5	VSS		VDD –1.5V	V
Internal reference voltage	VREF	"-" inputs of CMP2, CMP3, CMP4		4.5 to 5.5	2/3VDD –0.02	2/3VDD	2/3VDD +0.02	
AMP input voltage (Note9-2)	VAMIN	AMP1I		4.5 to 5.5	VSS		(VDD –1.5V) /Magnification of AMP	V
Offset voltage	VOFF(1)	CMP1IA, CMP1IB (CMP1)	Input common-mode voltage range	4.5 to 5.5			±20	mV
	VOFF(2)	CMP2I (CMP2), CMP4I (CMP4)	• Input common-mode voltage range • Including VREF error	4.5 to 5.5			±40	
	VOFF(3)	AMP1I (CMP3)	• AMP Input voltage range • Magnification of AMP1 is selected x8 by user option • Including VREF error	4.5 to 5.5			±28	
AMP output error	VAER	AMP2O	• AMP Input voltage range • Magnification of AMP1 is selected x8 by user option • Magnification of AMP2 is selected x1 by resister	4.5 to 5.5		±155	±200	mV
CMP1 response speed	tC1RT	CMP1O(P30)	• Input common-mode voltage range • Input amplitude=100mV • Over drive=50mV	4.5 to 5.5		200		ns
CMP3 response speed (Note9-3)	tC3RT	PPGO	• Magnification of AMP1 is selected x8 by user option • AMP1I rising timing • AMP1I=(VREF±100mV)/8 • See Fig. 10.	4.5 to 5.5		600		
CMP4 response speed	tC4RT	PPGO	• CMP4I rising timing • CMP4I=VREF±50mV • See Fig. 10.	4.5 to 5.5		200		

Note9-1 : When V_{DD}=5V, the comparison input voltage is effective from 0 to 3.5V.

Note9-2 : Magnification of AMP= Magnification of AMP1× Magnification of AMP2

When V_{DD}=5V, magnification of AMP1 to ×8 magnification of AMP2 to ×1, the AMP input voltage is effective from 0 to 0.4375V.

Note9-3 : PPGO have a delay of 1/6tCYC to 1/2tCYC from CMP1O falling timing for synchronization with system clock, when the pulse start delay setup register (ADDRESS: FE92H, FE93H) is set to 000H.

10. Consumption Current Characteristics at Ta=–40 to +85°C, $V_{SS}1$= $V_{SS}2$=0V

Parameter	Symbol	Pin/Remarks	Conditions	VDD[V]	Specification min.	typ.	Max.	unit
Normal mode consumption current (Note 10-1) (Note 10-2)	IDDOP(1)	VDD1	• FmCF=12 MHz ceramic oscillation mode • System clock set to 12 MHz side • Internal Low speed and Medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	4.5 to 5.5		8.7	16	mA
	IDDOP(2)		• FmCF=4 MHz ceramic oscillation mode • System clock set to 4 MHz side • Internal Low speed and Medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	4.5 to 5.5		4.4	8.7	
	IDDOP(3)		• CF oscillation low amplifier size selected. (CFLAMP=1) • FmCF=4 MHz ceramic oscillation mode • System clock set to 4 MHz side • Internal Low speed and Medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/4 frequency division ratio	4.5 to 5.5		2.6	4.8	
	IDDOP(4)		• FsX'tal=32.768 kHz Crystal oscillation mode • Internal Low speed RC oscillation stopped. • System clock set to internal Medium speed RC oscillation. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		2.1	3.8	
	IDDOP(5)		• FsX'tal=32.768 kHz crystal oscillation mode • Internal Low speed and Medium speed RC oscillation stopped. • System clock set to 8MHz with Frequency variable RC oscillation • 1/1 frequency division ratio	4.5 to 5.5		6.7	11.3	
	IDDOP(6)		• External FsX'tal and FmCF oscillation stopped. • System clock set to internal Low speed RC oscillation. • Internal Medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	4.5 to 5.5		1.6	2.6	
	IDDOP(7)		• FsX'tal=32.768 kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal Low speed and Medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		1.6	2.6	

Parameter	Symbol	Pin/remarks	Conditions		Specification			
				VDD[V]	min.	typ.	max.	unit
HALT mode consumption current (Note 10-1) (Note 10-2)	IDDHALT(1)	VDD1	• HALT mode • FmCF=12 MHz ceramic oscillation mode • System clock set to 12 MHz side • Internal Low speed and Medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	4.5 to 5.5		4.4	8.7	mA
	IDDHALT(2)		• HALT mode • FmCF=4 MHz ceramic oscillation mode • System clock set to 4 MHz side • Internal Low speed and Medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	4.5 to 5.5		2.9	5.5	
	IDDHALT(3)		• HALT mode • CF oscillation low amplifier size selected. (CFLAMP=1) • FmCF=4 MHz ceramic oscillation mode • System clock set to 4 MHz side • Internal Low speed and Medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/4 frequency division ratio	4.5 to 5.5		2.2	3.9	
	IDDHALT(4)		• HALT mode • FsX'tal=32.768 kHz crystal oscillation mode • Internal Low speed RC oscillation stopped. • System clock set to internal Medium speed RC oscillation • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		1.9	3.1	
	IDDHALT(5)		• HALT mode • FsX'tal=32.768 kHz crystal oscillation mode • Internal Low speed and Medium speed RC oscillation stopped. • System clock set to 8MHz with Frequency variable RC oscillation • 1/1 frequency division ratio	4.5 to 5.5		3.3	5.9	
	IDDHALT(6)		• HALT mode • External FsX'tal and FmCF oscillation stopped. • System clock set to internal Low speed RC oscillation. • Internal Medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	4.5 to 5.5		1.5	2.5	
	IDDHALT(7)		• HALT mode • FsX'tal=32.768 kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal Low speed and Medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		1.6	2.6	

Parameter	Symbol	Pin/remarks	Conditions		Specification			
				VDD[V]	min.	typ.	max.	unit
HOLD mode consumption current (Note 10-1) (Note 10-2) (Note 10-3)	IDDHOLD	VDD1	HOLD mode • FsX'tal=32.768 kHz crystal oscillation mode • LVD option selected	4.5 to 5.5		1.5	2.6	mA

Note10-1 : Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.
Note10-2 : The consumption current values do not include operational current of LVD function if not specified.
Note10-3 : AMP/CMP circuit is operating in HOLD mode.

11. F-ROM Programming Characteristics at Ta=+10 to +55°C, $V_{SS}1$= $V_{SS}2$=0V

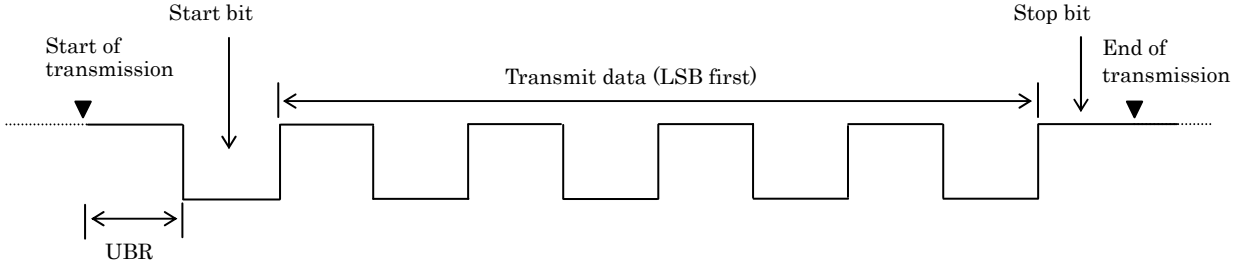
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				VDD[V]	min.	typ.	max.	unit
Onboard programming current	IDDFW(1)	VDD1	• Only current of the Flash block.	4.5 to 5.5		5	10	mA
Programming time	tFW(1)		• Erasing time	4.5 to 5.5		20	30	ms
	tFW(2)		• Programming time			40	60	µs

12. UART (Full Duplex) Operating Conditions at Ta=–40 to +85°C, $V_{SS}1$= $V_{SS}2$=0V

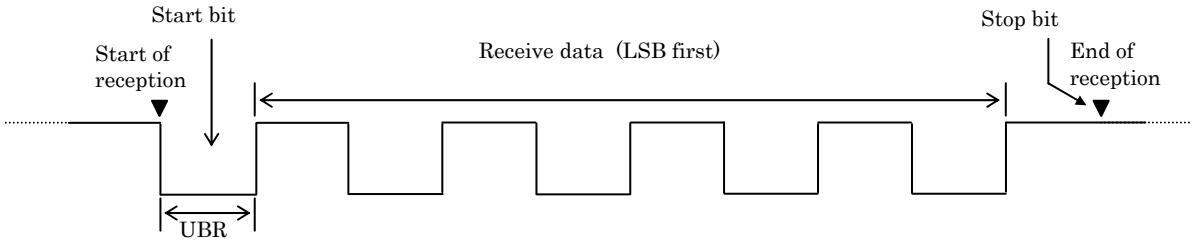
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				VDD[V]	min.	typ.	max.	unit
Transfer rate	UBR	UTX(P20) URX(P21)		4.5 to 5.5	16/3		8192/3	tCYC

Data length : 7/8/9 bits (LSB first)
Stop bits : 1 bit(2-bit in continuous data transmission)
Parity bits : None

Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data=55H)



Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data=55H)



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a ON Semiconductor-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1. Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

- CF oscillation normal amplifier size selected (CFLAMP=0)

■ **MURATA**

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		Typ [ms]	Max [ms]	
12MHz	SMD	CSTCE12M0G52-R0	(10)	(10)	Open	680	4.5 to 5.5	0.1	0.5	Internal C1,C2
10MHz	SMD	CSTCE10M0G52-R0	(10)	(10)	Open	680	4.5 to 5.5	0.1	0.5	
	LEAD	CSTLS10M0G53-B0	(15)	(15)	Open	680	4.5 to 5.5	0.1	0.5	
8MHz	SMD	CSTCE8M00G52-R0	(10)	(10)	Open	1k	4.5 to 5.5	0.1	0.5	
	LEAD	CSTLS8M00G53-B0	(15)	(15)	Open	1k	4.5 to 5.5	0.1	0.5	
6MHz	SMD	CSTCR6M00G53-R0	(15)	(15)	Open	1.5k	4.5 to 5.5	0.1	0.5	
	LEAD	CSTLS6M00G53-B0	(15)	(15)	Open	1.5k	4.5 to 5.5	0.1	0.5	
4MHz	SMD	CSTCR4M00G53-R0	(15)	(15)	Open	1.5k	4.5 to 5.5	0.2	0.6	
	LEAD	CSTLS4M00G53-B0	(15)	(15)	Open	1.5k	4.5 to 5.5	0.2	0.6	

- CF oscillation low amplifier size selected (CFLAMP=1)

■ **MURATA**

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		Typ [ms]	Max [ms]	
4MHz	SMD	CSTCR4M00G53-R0	(15)	(15)	Open	1k	4.5 to 5.5	0.2	0.6	Internal C1,C2
		CSTCR4M00G53095-R0	(15)	(15)	Open	1k	4.5 to 5.5	0.2	0.6	
	LEAD	CSTLS4M00G53-B0	(15)	(15)	Open	1k	4.5 to 5.5	0.2	0.6	
		CSTLS4M00G53095-B0	(15)	(15)	Open	1k	4.5 to 5.5	0.2	0.6	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Figure 3).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a ON Semiconductor-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2. Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

■ EPSON TOYOCOM

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		Typ [s]	Max [s]	
32.768kHz	SMD	MC-306	8pF	8pF	Open	0Ω	4.5 to 5.5	1.00s	1.50s	Applicable CL value = 7.0pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 3).

Note : The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

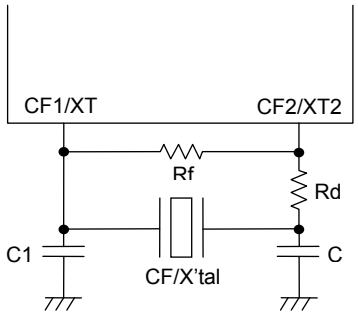


Figure 1. CF and XT Oscillator Circuit

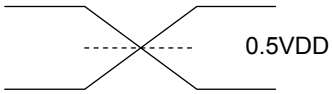
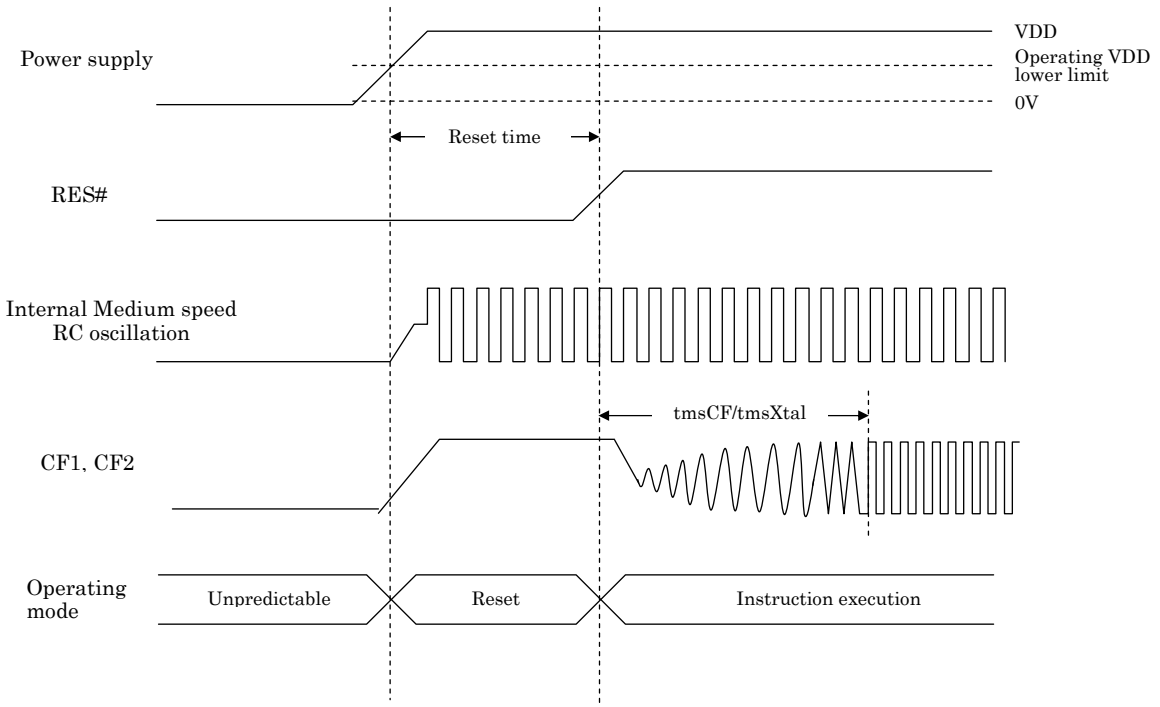
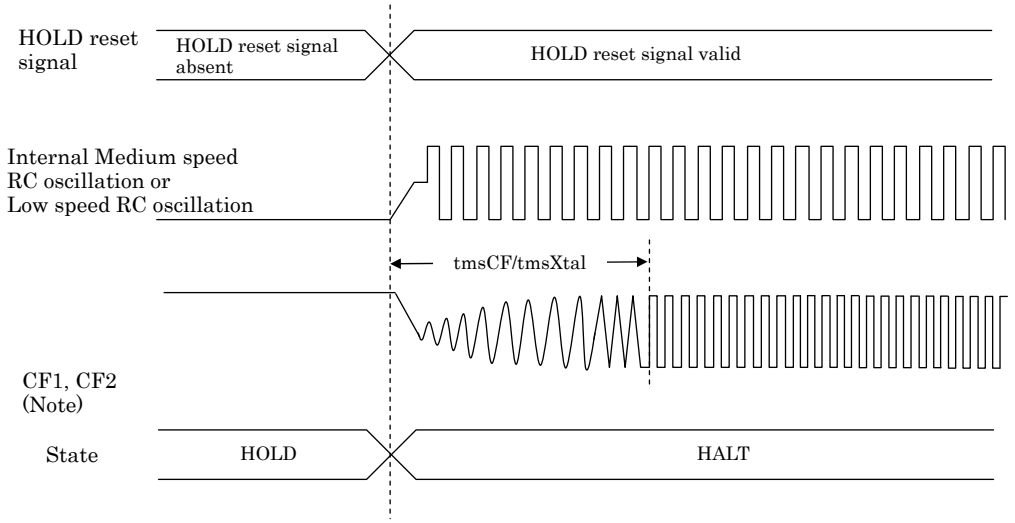


Figure 2. AC Timing Measurement Point



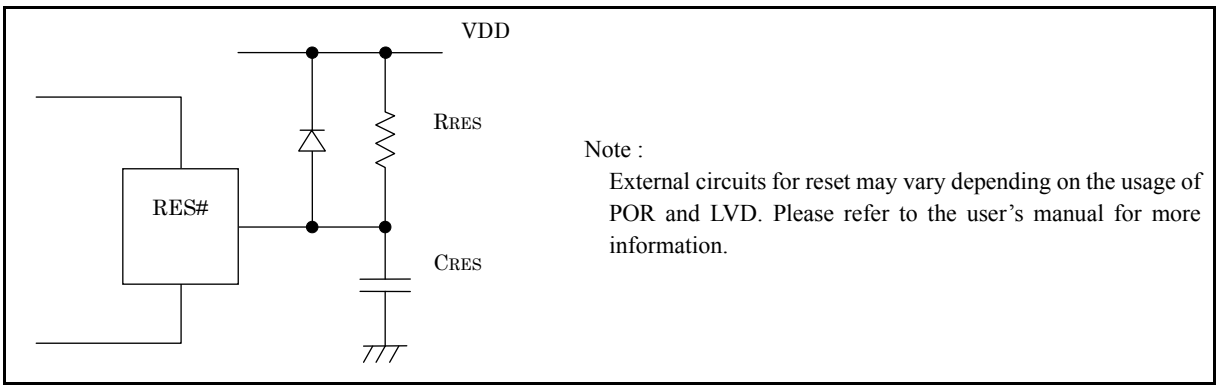
Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Note : External oscillation circuit is selected.

Figure 3. Oscillation Stabilization Times



Note :
External circuits for reset may vary depending on the usage of POR and LVD. Please refer to the user's manual for more information.

Figure 4. Reset Circuit

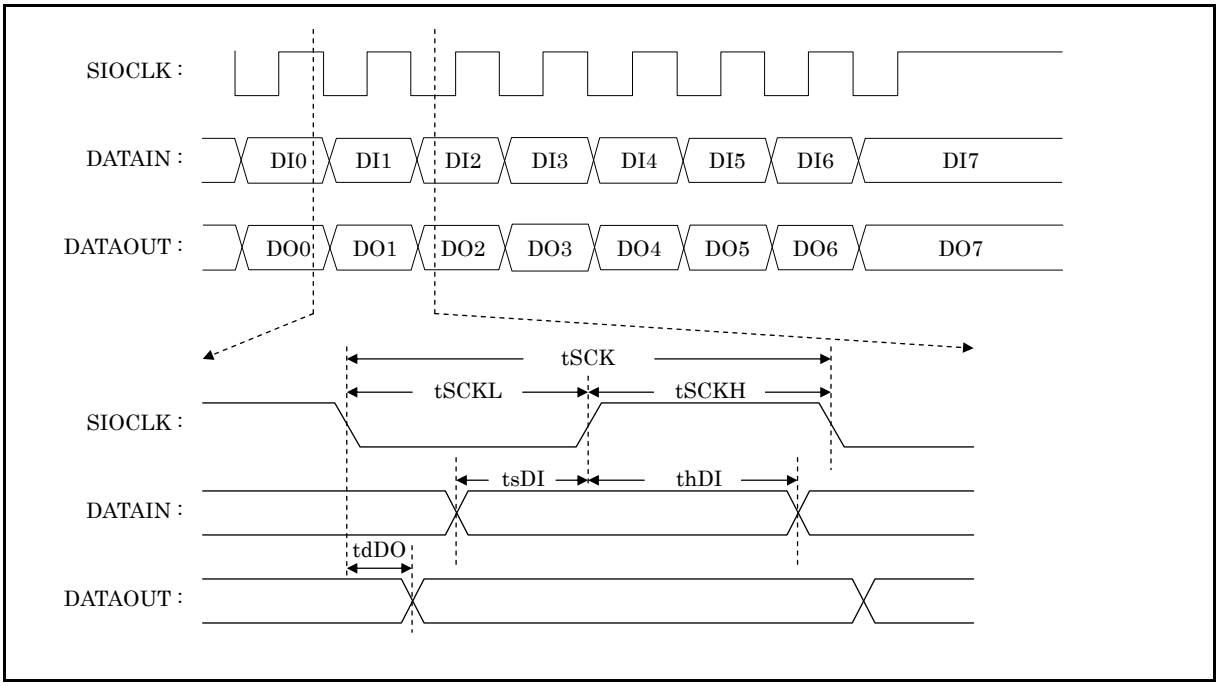


Figure 5. Serial I/O Output Waveforms

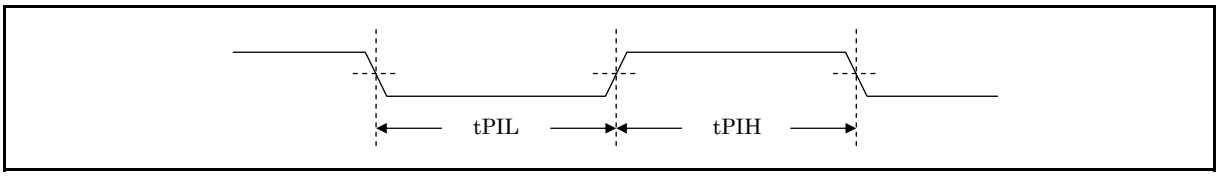


Figure 6. Pulse Input Timing Signal Waveform

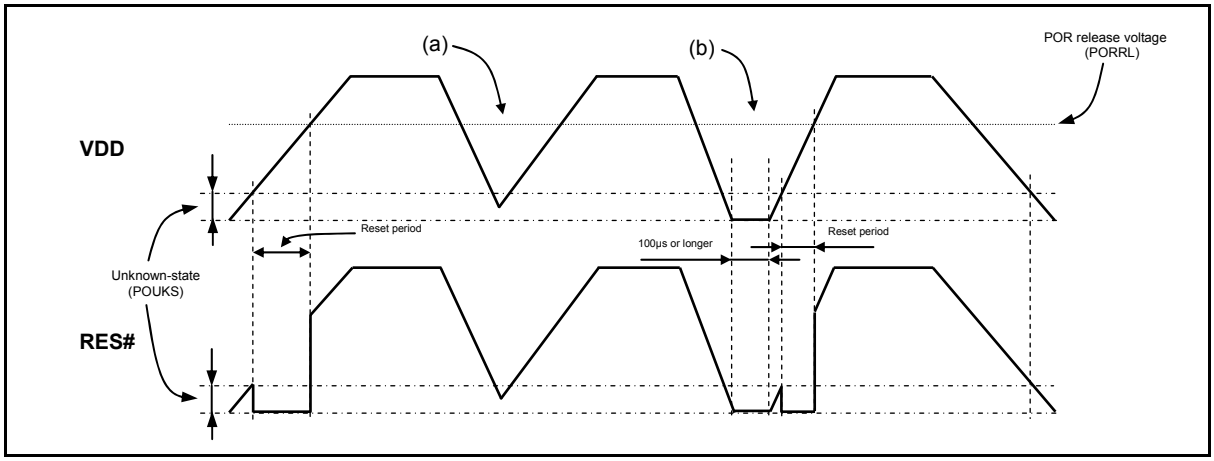


Figure 7. Waveform observed when only POR is used (LVD not used)
(RESET pin: Pull-up resistor R_{RES} only)

- The POR function generates a reset only when power is turned on starting at the VSS level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the VSS level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit.
- A reset is generated only when the power level goes down to the VSS level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

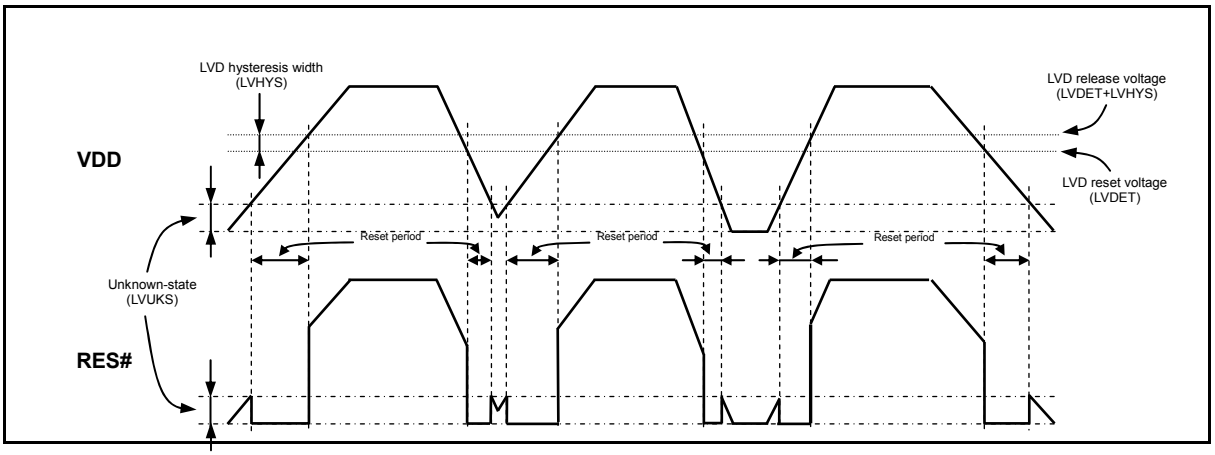


Figure 8. Waveform observed when both POR and LVD functions are used
(RESET pin: Pull-up resistor R_{RES} only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

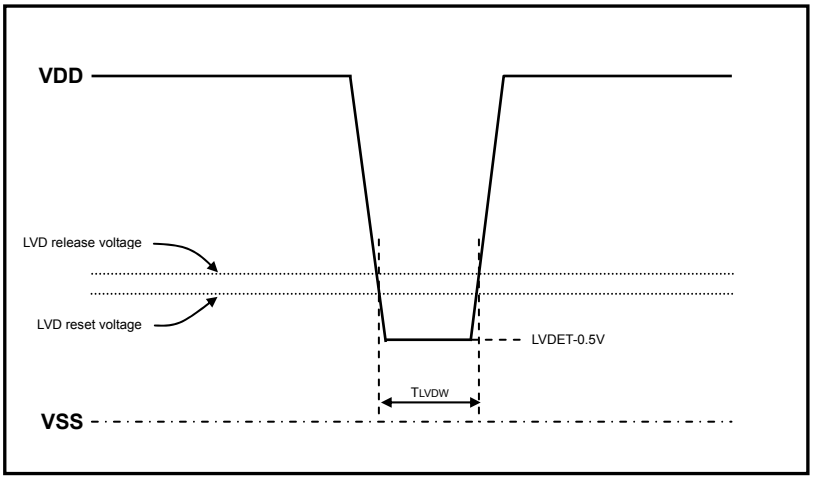


Figure 9. Low voltage detection minimum width
(Example of momentary power loss / Voltage variation waveform)

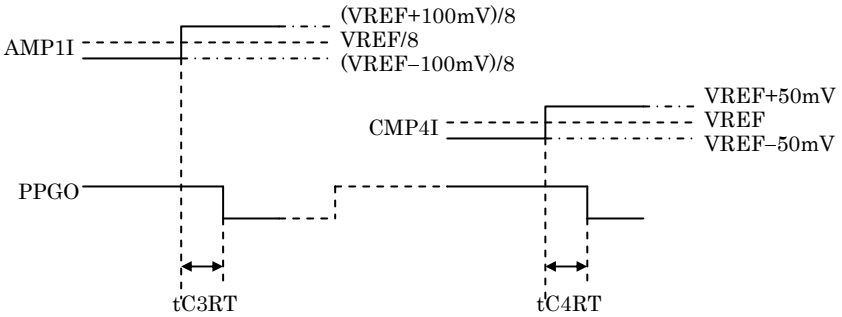


Figure 10. CMP response time

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC87F2L08AU-DIP-E	DIP30SD(400mil) (Pb-Free)	20 / Fan-Fold